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Defect analysis of strained silicon on thin strain-relaxed buffer layers for high mobility transistors

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Abstract
The electrical activity of defects present in strained silicon (SSi) on thin strain-relaxed $Si_{1-x}Ge_x$ buffer layers (SRBs) is evaluated using deep submicron CMOS compatible n^+/p and p^+/n shallow junctions. Strain relaxation has been achieved here by introducing a thin carbon-rich layer in an otherwise uniform $Si_{0.78}Ge_{0.22}$ epitaxial layer, resulting in an SRB thickness of 248 or 348 nm and processing compatible threading dislocation densities in the range of a few 10^6 cm^{-2}. From a combination of electrical measurements (current– and capacitance–voltage; microwave absorption (MWA) recombination lifetime) and microscopic techniques (electron-beam-induced current; emission microscopy), it is concluded that generation centres associated with the C layer can play an important role. Their electrical activity is shown to depend strongly on the relative position of the C-doped layer with respect to the junction depth. The type of well dopant (implantation) also has a strong impact on the electrical activity of the different defect types present in the epitaxial layers. It is generally found that the 348 nm junctions show a lower reverse current at practical operation temperatures and voltages, while the p^+/n diodes exhibit a better performance compared with their n^+/p counterparts.

1. Introduction

There is currently a strong interest in the development of deep submicron CMOS on so-called high-mobility substrates, e.g., germanium or strained silicon [1]. The ultimate goal is to benefit from the strain-enhanced mobility to boost the device and circuit performance.

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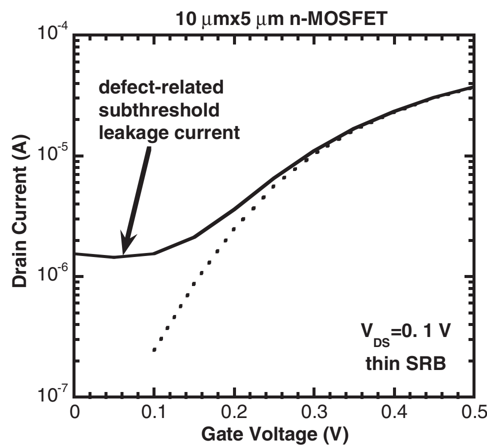

Figure 1. Input characteristics in linear operation (drain voltage V_{DS} = 0.1 V) for two 10 μm × 5 μm n-MOSFETs fabricated on a strained silicon wafer with a thin SRB layer. The full line corresponds to a device with a high extended-defect-related subthreshold leakage current.

In the case of strained silicon (SSi), a thin layer of silicon (∼10 nm) is grown on top of a strain-relaxed $Si_{1-x}Ge_x$ buffer (SRB). Traditionally, rather thick (∼1 μm) so-called virtual substrates are grown, whereby the percentage of Ge is increased stepwise from $x = 0$ to the desired value, which is typically between 20 and 30%. Alternative approaches have been recently proposed [2–6] to lower the SRB thickness. This should reduce the wafer cost and improve its thermal properties, since SiGe has a rather poor thermal conductivity. In this way, SRBs in the range of 300–400 nm can be produced with a device-quality threading dislocation (TD) density ($N_{TD} \sim 10^6$ cm^{-2}) [7]. However, as demonstrated recently, the issue of the electrical activity of TDs and misfit dislocations remains of concern. It has for example been demonstrated that the presence of dislocations near the channel region can cause a diffusion of dopants from source to drain, creating a local short and a strong enhancement of the off-state leakage current [8, 9]. An example is given in figure 1, showing the input drain current (I_D)—gate voltage (V_{GS}) characteristics of two SSi 10 μm × 5 μm n-MOSFETs, one exhibiting a large off-state leakage current at $V_{GS} = 0$ V. Wide transistors are particularly prone to this leakage mechanism as the chance of intersection with a threading dislocation is proportionally higher.

It is the aim of this paper to investigate electrically active defects in thin SRBs, fabricated by implementing a thin carbon-doped layer in a constant composition $Si_{0.78}Ge_{0.22}$ layer to provide nucleation sites for dislocations and schematically represented in figure 2 [6]. This investigation is carried out by a number of electrical and structural characterization techniques, applied to shallow junctions fabricated in the strained silicon substrates.

2. Experimental details

Shallow junction diodes, compatible with a deep submicron CMOS process, have been fabricated in 8 nm SSi grown on 248 or 348 nm SRB layers with a Ge concentration of 22%. In the context of this paper, the two substrates will be termed ‘thin’ and ‘thick’. Epitaxial layers have been grown in an ASM 2000 epsilon reactor, as described in more detail elsewhere [7]. A corresponding cross sectional transmission electron microscopy (TEM) image is given in figure 3, showing good layer quality. The TD density for this batch of material was estimated

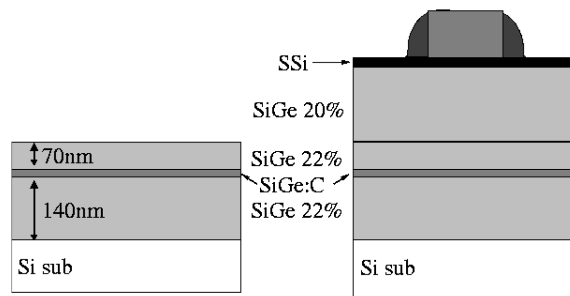

Figure 2. Schematic view of the strained Si and SiGe virtual substrates after the first growth step (left) and after the third step (right).

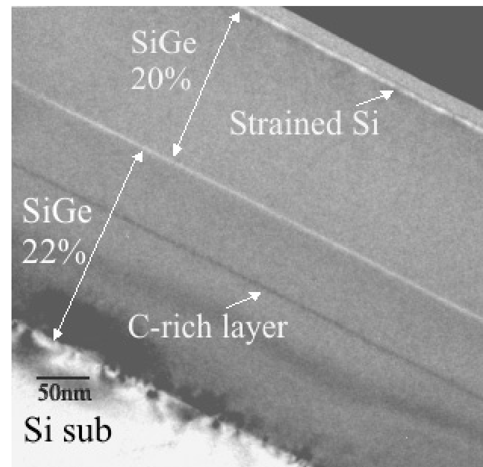

Figure 3. XTEM micrograph of the strained Si buffer layers.

to be $\sim 3 \times 10^6$ cm^{-2}, from defect etching and counting under an optical microscope. Three types of defects are typical for our SSi material: misfit dislocation at the silicon substrate/SRB and at the SSi/SRB interfaces, individual threading dislocations and pile-ups of threading dislocations.

After the layer deposition, a box isolation scheme was used to pattern junctions with a total area of 10^5 μm^2. Both p$^+$/n and n$^+$/p junctions were fabricated by standard well, channel and highly doped drain (HDD) implantations: 2 keV B to a dose of 2×10^{15} cm^{-2} (p$^+$/n) and 20 keV As to a dose of 4×10^{15} cm^{-2} (n$^+$/p), respectively. Dopant activation was achieved by conventional '0 s' spike annealing at 1000 °C. Nickel silicidation was used to lower the contact resistance. A junction depth (d_j) of 50 nm was derived from process simulation, which was in reasonable agreement with the d_j found from secondary ion mass spectrometry (SIMS). The resulting geometry of the junctions in the thin and thick SRB wafers is schematically represented in figure 4. Important in this figure is the relative position of the C-doped layer with respect to the built-in space charge region (SCR): in the case of the thin layer, the C layer is in the SCR or in its close proximity, already at 0 V, while it is clearly outside the SCR for the thick layers. As will be detailed below, this has serious consequences for the electrical characteristics of the junctions. Reference diodes on standard silicon wafers were also processed.

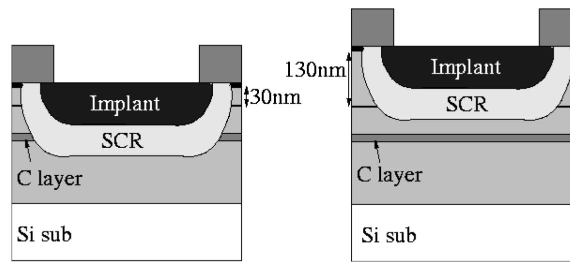

Figure 4. Position of the implanted junctions for the thin (left) and thick (right) buffer layers, estimated at 0 V bias.

By a combination of current–voltage (I–V) and capacitance–voltage (C–V) measurements, the impact of the substrate quality on the diode leakage current was investigated, following the procedures outlined elsewhere [10, 11]. Initially, automatic measurements have been performed on the leakage current at a fixed reverse bias on all available diode structures across the 200 mm diameter wafers, providing an idea on the yield and the average value. For detailed I–V and C–V measurements as a function of temperature, a few typical devices per wafer were selected.

It should be remarked here that the use of the p–n junction characteristics as a materials characterization tool has the advantage that the substrates receive most of the front-end processing, resulting in a device structure whereof the physics is reasonably simple to be exploited for that purpose. Moreover, a junction can be used for other well established techniques, like deep level transient spectroscopy (DLTS), electron beam induced current (EBIC) or emission microscopy (EMMI). Here, room temperature EBIC has been performed on reverse-biased junctions, employing a beam energy of 3 keV on a JEOL JEM-840 scanning electron microscope. EMMI analyses were performed on non-silicided junctions mounted in a Hypervision-Visionary II photoemission microscope, as described previously [12]. Finally, microwave absorption (MWA) lifetime measurements have been performed on the processed wafers. Further details of the MWA technique can be found in [13]. In order to reveal the lifetime of the near-surface virtual substrate and strained layer, three excitation wavelengths have been used, namely 350, 532 and 1064 nm. The decay of the excess carriers was monitored by two digital oscilloscopes: a JA4C122 with a time resolution of 0.1 μs and a Tektronix TDS5104 with a resolution of 1 ns.

3. Results and discussion

Figure 5 clearly illustrates the drastic impact of the virtual substrate on the J–V characteristics of the diodes: a strong increase in both the forward and reverse current is observed, which is most pronounced for the thin SRBs, for not too high absolute values of the bias. Note that, according to figure 4, the SCR expands mainly in the SiGe layer, which corresponds to a smaller bandgap compared with silicon. For $x = 0.22$ and relaxed SiGe, a bandgap energy of 1.0 eV has been calculated, yielding an intrinsic carrier concentration (n_i) at 300 K of 9.9×10^{10} cm^{-3}, which is about four times higher than the silicon value. As the reverse generation current is proportional to n_i, we can expect a roughly four times higher reverse generation current in the SRB junctions for the same defect density and depletion width. This cannot, however, explain the four to five orders of magnitude increase observed in figure 5. Neglecting differences in well profiles, it is clear that the relaxed buffer layers contain a high density of defects, which act

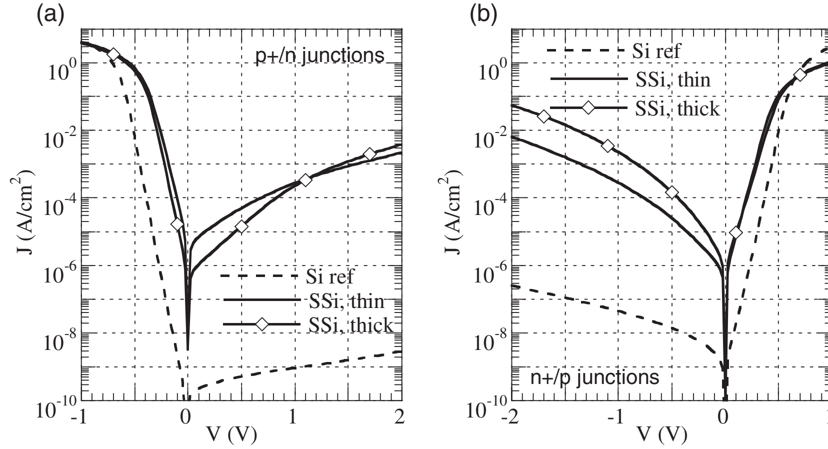

Figure 5. Current density versus voltage characteristics of the p^+/n diodes (a) and the n^+/p diodes (b), on the different substrate types under study ($T = 300$ K).

as generation centres and strongly reduce the carrier lifetime. In the next sections, the results of the different analysis techniques will be described and discussed. The picture emerging from this is that besides the TD density, which is the same for both types of SRB wafers, the presence of the C layer is thought to play a crucial role. It will be shown that associated with it there exists a high local density of electrically active defects, which have a different impact in the thin compared with the thick SRB material. An additional factor defining the leakage current appears to be the type of well dopant (p or n).

3.1. Diode characteristics

Comparing figures 5(a) and (b), a few interesting trends can be derived. Besides the clearly higher reverse current density (J_R) for the SRB devices, there are also differences between the thin and thick case. For the p^+/n junctions, the thick devices show a nearly one decade smaller J_R at a reverse bias $V_R < 1$ V, which is maintained up to the highest temperatures studied (500 K) [10]. Another noteworthy fact is that the thick p^+/n junctions show a steeper slope in their reverse current characteristic. The situation is opposite for the n^+/p diodes at 300 K (figure 5(b)), where a lower J_R is found for the thin SRB devices. However, the latter diodes exhibit a much more pronounced temperature dependence so that at the expected circuit operation temperature (~100 °C) and bias (~$V_R = 1$ V) of the strained silicon technology the thick SRB diodes exhibit a smaller J_R [10].

One way to obtain a better insight into the leakage current mechanisms is by studying the temperature dependence of the reverse current at fixed V_R, which has been reported in detail in [10]. The main observation was that for the case of the thin SRBs the activation energy (E_a) is markedly smaller than the expected band gap of ~1 eV, for the whole temperature range examined, up to 250 °C and this for both n^+/p and p^+/n devices. The conclusion was that the leakage current is generated by deep levels in the SCR. For the thick SRBs, on the other hand, the activation energy reached about 1 eV at higher temperatures, indicating the dominance of the diffusion mechanism. Near room temperature, E_a was lower than expected, suggesting the dominance of tunnelling or another electric field assisted leakage current mechanism. It has also been observed that the reverse current follows a V^ν law, with ν between 3 and 5, which is in line with field-assisted breakdown [14, 15].

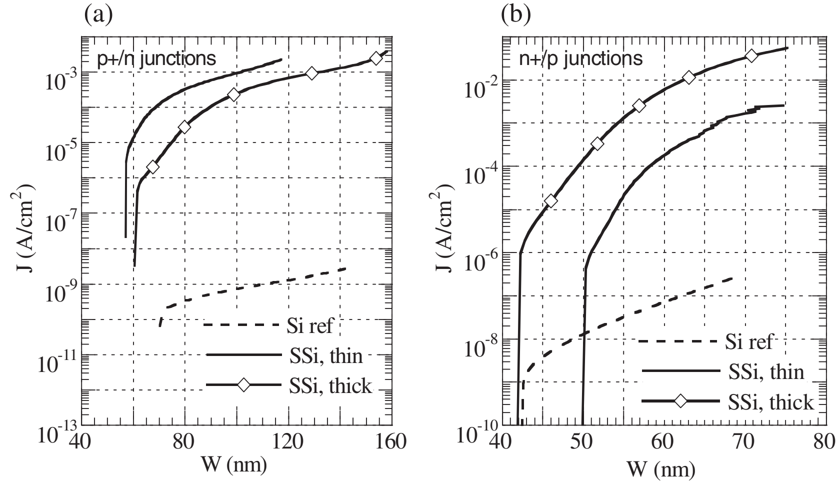

Figure 6. Reverse current density versus depletion width of the p^+/n diodes (a) and the n^+/p diodes (b), on the different substrate types under study ($T = 300$ K).

Another way to separate different leakage current contributions is by plotting J_R versus the depletion width W [16], whereby the latter can be derived from the measured C–V plot, according to

$$W = \varepsilon_{\mathrm{SiGe}} A/C \tag{1}$$

with $\varepsilon_{\mathrm{SiGe}}$ the permittivity of $Si_{0.78}Ge_{0.22}$ and A the junction area. If thermal generation dominates, one expects the J_R–W plot to be a straight line with slope given by qn_i/τ_g and intercept determined by the diffusion leakage current density J_{diff}; q is the elementary charge and τ_g the generation lifetime. This enables the extraction of the generation lifetime. In practice, however, the J–W dependence in figures 6(a) and (b) is much more complicated, even for the reference silicon devices. This points to the importance of field-assisted generation mechanisms, like the Poole–Frenkel effect or trap-assisted tunnelling [11, 17]. As a rough first-order estimate of the effective generation lifetime, one can define

$$\tau_{\mathrm{geff}} = qn_i[\partial J_R/\partial W]^{-1} \tag{2}$$

which yields at $V_R = 0$ V (at the edge of the built-in SCR) a value of ~5 ns (thick p^+/n) and 0.5 ns (thin p^+/n) and ~1 ns (thick and thin n^+/p), respectively.

According to Giovane *et al* [18], the generation lifetime associated with TDs in SiGe p–i–n diodes is given by:

$$\tau = 1/(\sigma_n v_{\mathrm{th}} N_{\mathrm{TD}} n_D) \tag{3}$$

with σ_n the capture cross section for electrons (4×10^{-12} cm^2); v_{th} the thermal velocity (1.17×10^7 cm s^{-1} at 300 K); N_{TD} the dislocation density (3×10^6 cm^{-2}) and n_D the number of traps per length of dislocation (10^6 cm^{-1}). This leads to a value of 7.1 ns, which is of the same order as the effective lifetimes derived above. It is clear, however, that, particularly for the thin SRB material, the effective lifetime at zero bias (lowest average electric field) is markedly below the value predicted by equation (3). This suggests that other generation centres, for instance associated with the C layer in the built-in SCR (figure 4(a)), reduce the generation lifetime and, hence, enhance the leakage current.

A further qualitative argument in favour of the latter interpretation—at least in the case of the p^+/n diodes of figure 5(a)—is the different slope $\partial J/\partial V$ found for the thick and thin SRB

layers. The higher starting value at 0 V suggests a high density of leakage-generating defects already present in the built-in SCR. However, the steeper slope for the thick SRB junction compared with the thin one suggests a higher defect density when the SCR region widens upon increasing the reverse bias. This is consistent with the position of the C layer in figure 4, inside the built-in SCR for the thin and outside for the thick SSi substrate. The situation of the thin SRB junction is in fact very similar to the case of pre-amorphization-induced end-of-range defects in p^+/n junctions studied by Brotherton and co-workers [19, 20] and can most likely be modelled along the same lines.

A final interesting feature noticeable in figure 6(a) is the shift of the built-in SCR width to lower values for the SRB p^+/n diodes, the lowest value corresponding to the thin SRB layer. Apparently, the C-rich layer seems to drag the n-well closer to the junction. In contrast, for the n^+/p junctions a wider built-in SCR is discerned in figure 6(b) for the thin SRB diodes. This could be related to the impact of SiGe, on the one hand, and C, on the other, on the diffusion behaviour of the n- or p-type well dopants. It is well known that for example arsenic diffusivity is enhanced in SiGe [21], while the B diffusivity is retarded [22]. At the same time, C is useful in the suppression of the self-interstitial-mediated transient enhanced diffusion of boron [23]. Moreover, initial SIMS analysis has indicated that the junction depth is also different for the different substrates studied, so that it is not clear for the moment whether the change in the width of the SCR is due to a change in the well profile by dopant diffusion or whether it is related to the movement of the junction relative to the well profiles.

3.2. EBIC and EMMI imaging

Figure 7 represents the EMMI images recorded for a reference (a), a thick (b) and a thin (c) SRB n^+/p junction, respectively. They are so-called integrated images, obtained after a voltage sweep from 1 V in forward operation to −15 V reverse bias. The bright spots in the pictures represent local breakdown spots, generally associated with an extended-defect site or high electric field region, where hot carriers lose energy by visible-light photon emission [11, 14, 15, 24, 25]. For the reference devices, junction breakdown occurs around 6.6 V, while light emission was preferentially observed near the edge of the devices (figure 7(a)). It demonstrates the absence of defective sites in the interior area of the standard silicon diodes, where breakdown starts at the high electric field regions near the oxide isolation periphery of the junctions.

In the thick SRB n^+/p junction, on the other hand, the breakdown spots were uniformly distributed across the surface of the diodes, with a density much higher than N_{TD} (figure 7(b)). In contrast, the thin SRBs show the electrical activity of the misfit dislocation network at the bottom interface, in figure 7(c) together with a more or less uniform background glow. The appearance of a uniform brightness across the junction area points to a field-assisted tunnelling breakdown, most likely related to the presence of defects at the C-rich layer [14, 15]. The fact that a high density of breakdown spots is observed in figure 7(b) is also in line with the low activation energy of the leakage current, pointing to tunnelling in a local high field region, probably around small precipitates or defect clusters. These can be created by the interaction between the C-rich layer and the implantation damage formed during the well implant, leading probably to small self-, C- or B-interstitial clusters, that may be either electrically active or create high local electric fields.

Apparently, the C-related layer is somewhat less active (less bright) in the thin SRB junctions, which could be explained by the fact that the C layer is closer to the junction. Analogous to the case of the end-of-range damage band of defects [20, 21], when the C layer is near the electrical junction, its generation current will be reduced by the injected minority

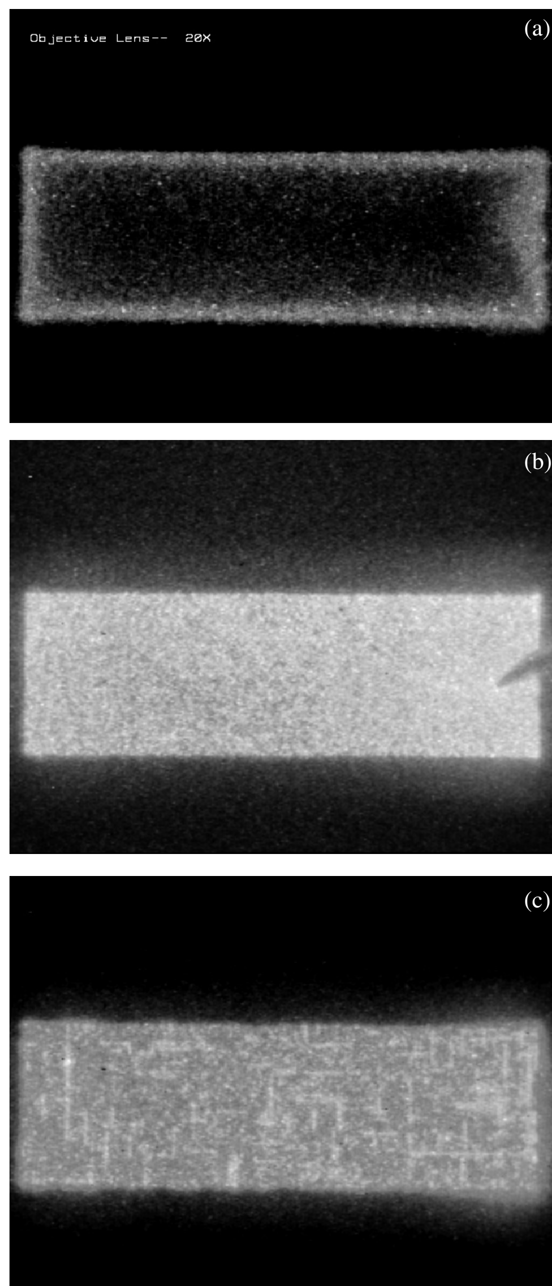

Figure 7. EMMI micrographs corresponding to 10^5 μm^2 n^+/p junctions fabricated in (a) a reference silicon wafer; (b) a thick SRB wafer and (c) a thin SRB wafer.

carriers, while this is not the case for the thick SRB material. The observation of microplasma breakdown at the misfit dislocations in the thin SRB junctions can be understood by considering the closer proximity of the silicon substrate/SRB interface to the junction (100 nm closer than for the thick SRB case, figure 4), so that it can be depleted by a reverse bias of −15 V. On the other hand, the SSi/SRB misfits are at the same distance in both cases and probably

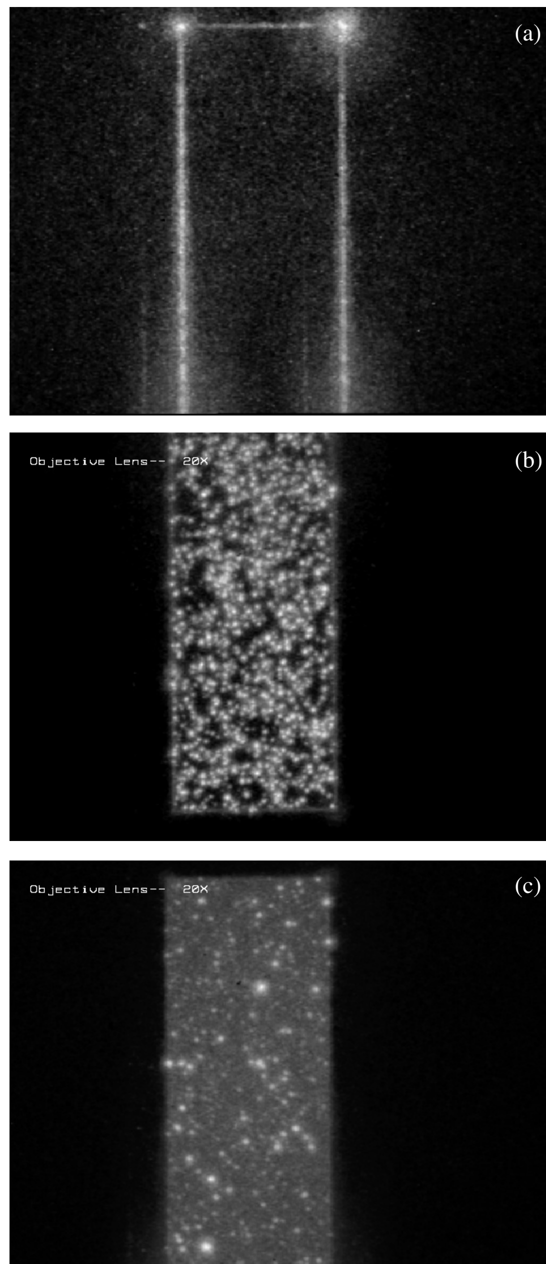

Figure 8. EMMI micrographs corresponding to 10^5 μm^2 p^+/n junctions fabricated in (a) a reference silicon wafer; (b) a thick SRB wafer and (c) a thin SRB wafer.

cannot be depleted by the reverse bias, so that we can safely rule them out as the origin of the microplasma defects in figure 7(c). It should finally be remarked that the EMMI analysis on the n^+/p junctions does not reveal electrical activity of the threading dislocations.

A different picture is obtained from the breakdown imaging of the p^+/n junctions, shown in figure 8. Again, the reference silicon diode breaks down preferentially at the edges and in

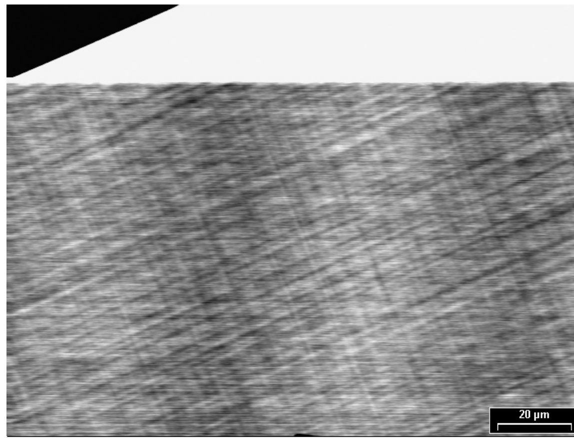

Figure 9. EBIC image of a thick SRB p^+/n junction diode at a beam energy of 3 keV and $T = 300$ K, showing the misfit dislocation network.

the corners, as expected. However, this time, the breakdown sites are randomly distributed over the area for both the thin and thick SRB layers, in figures 8(b) and (c), respectively. The breakdown spots do not resemble the misfit lines as in figure 7(c), and they are not uniformly distributed as in figure 7(b) for the thick SRB n^+/p junctions. They seem to occur in a clustered fashion or as random isolated spots. It is very probable that these breakdown sites correspond to microplasmas generated at individual threadings [15, 25] and dislocation pile-ups, known to be present in the starting material, from optical microscopy after preferential etching. Support for this is the agreement between the theoretical generation lifetime for threading dislocations derived from equation (3) and the experimental value extracted from the reverse current characteristics. From figures 7 and 8, it is concluded that the electrical activity of the different defect types not only depends on the layer structure (thickness) but also on the well doping type. Detailed analytical modelling is required to understand this different behaviour and the difference in the J_R–V characteristics of figures 5 and 6.

In an effort to gain more insight into the electrical activity of the extended defects, room-temperature EBIC measurements have been performed, whereof figure 9 is a typical result obtained on a thick SRB sample. It clearly demonstrates the recombination activity of the misfits, but no contrast due to TDs was found. In fact, according to a recent report, one can only expect to observe the EBIC contrast of clean TDs at lower temperature (e.g., 77 K) [26].

3.3. MWA lifetime analysis

As mentioned above, three excitation laser wavelengths and short (30 ps) laser pulses were applied to enable the separation of surface, near-surface and bulk recombination lifetime. The corresponding transients for the reference material (p^+/n) are represented in figure 10(a). It can be noticed that at bulk excitation (1064 nm) the carrier decay is nearly mono-exponential. At inhomogeneous short wavelength excitation, two components become obvious, where the initial excitation depth is 1 μm at 532 nm, and shorter for 350 nm. The latter two transients nearly coincide, evidencing that surface recombination prevails in the structure. From these transients, a bulk (Si substrate) recombination lifetime $\tau_b \geqslant 100$ μs and a surface recombination velocity $s \geqslant 100$ cm s^{-1} was derived.

In contrast, different MWA transients can be clearly revealed in the SRB n-well material, using the two short wavelength excitations, in figures 10(b) and (c). The effective lifetime

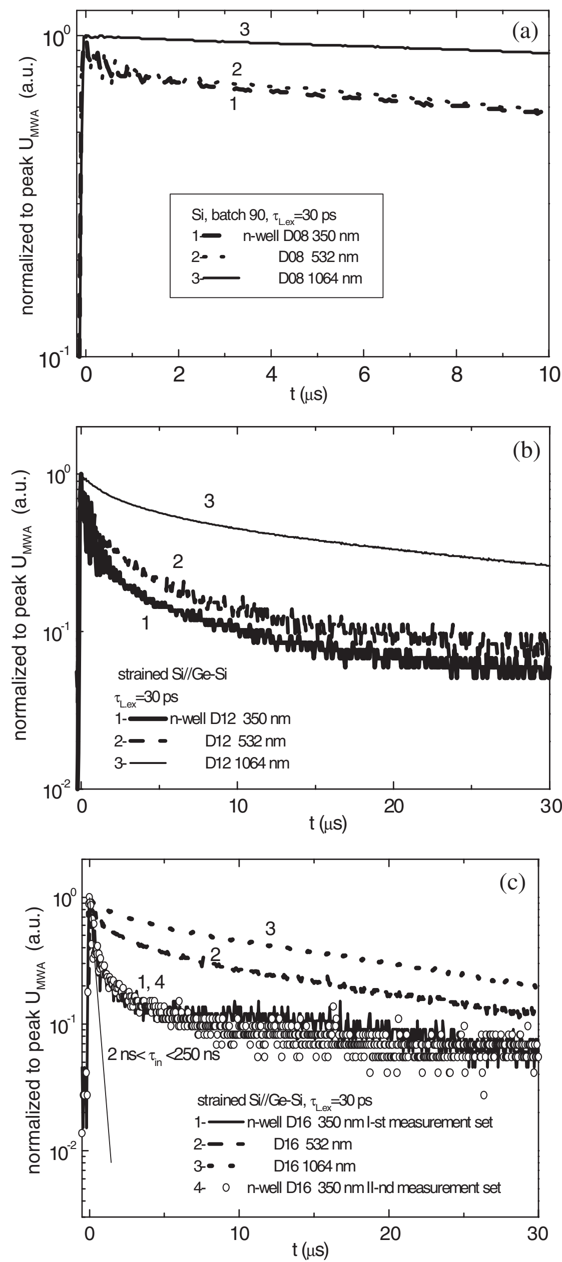

Figure 10. MWA transients for varying excitation wavelength, corresponding to p^+/n junctions fabricated in (a) a silicon reference wafer; (b) a thick SRB and (c) a thin SRB.

of the short decay constituent decreases and the MWA transient becomes fractured due to recombination in the top layers and due to domain spread, when carriers diffuse into the substrate, for the UV excitation employed. For the 532 nm excitation, the surface recombination prevails. The resulting near-surface effective lifetimes are summarized in table 1, showing higher values for the thin SRBs.

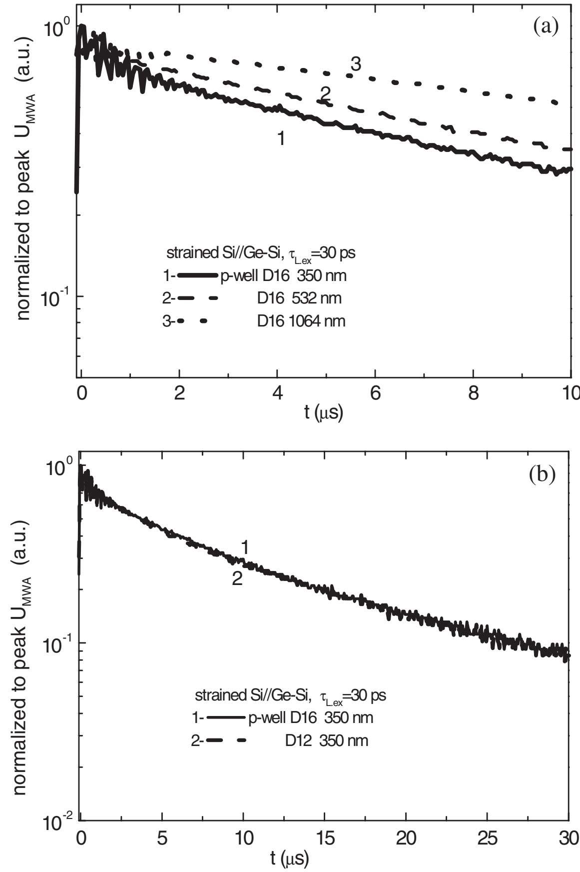

Figure 11. MWA transients in a p-well sample corresponding with (a) varying excitation wavelength (thick SRB layer), and comparison of decays in the thick and thin SRB wafers with p-well at 350 nm (b).

Table 1. Effective lifetimes attributed to the top structure.

Batch/sample	Well	τ_{in} (ns)
Thick SRB	n	27–170
Thin SRB	n	80–270
Thick SRB	p	300–530
Thin SRB	p	600–900

In the p-well samples, the effective lifetimes are longer than those in the n-well (figure 11(a)) and the difference between the decays at 532 and 350 nm is less. Moreover, the difference between the thick and thin SRB samples is less pronounced, as shown in figure 11(b) and table 1. This agrees to some extent with the similar effective generation lifetimes derived from the diode leakage currents, although the values for τ_{geff} were found to be much smaller ($\sim$1 ns), compared with the thick SRB p^+/n junctions.

It has been demonstrated in the past for GaAs epitaxial layers deposited on a silicon substrate that the recombination lifetime of the TDs is given by [27–29]

$$\tau_{TD} = 4/\pi^3 N_{TD} D. \tag{4}$$

In equation (4), D is the minority carrier diffusion length. Assuming for the time being a value of 10 cm^2 s^{-1} for D, we arrive at a $\tau_{TD} = 4.3$ ns. This is much smaller than the effective recombination lifetimes mentioned in table 1, although it is in reasonable agreement with the estimated (and measured) generation lifetimes, corresponding to equation (3).

On the other hand, the effective lifetime τ_{eff}, extracted from the MWA decay, can be phenomenologically approximated by the lifetime of the different processes of recombination at dislocations [30], $\tau_{TD} = 1/[f(\sigma_n, N_{TD}, v_{th})N_{TD}]$ (where σ_n and the potential barrier at the dislocation are dependent on the carrier density), the diffusion time into the depth of the structure, $\tau_{DII} = d^2/\pi^2 D$ (where d is the thickness of the top SiGe layer and the excitation pulse τ_L is short enough to satisfy $d > (D\tau_L)^{1/2}$), the perpendicular diffusion across the dislocation network $D_\perp = 4/\pi^3 N_{TD} D_\perp$, and the effective lifetime τ_b of the bulk and boundary recombination of the top layer. This implies that

$$\tau_{eff} = \Phi(\tau_{TD}, \tau_{DII}, \tau_{D\perp}, \tau_b) \tag{5}$$

which is a complicated function Φ of the N_{TD}, to be determined experimentally.

Currently, a more extensive MWA analysis is being undertaken, on starting material with different N_{TD}, in order to investigate the possible correlation between τ_{eff} from MWA and N_{TD}. However, from a comparison of the lifetimes in the thick and thin SRB materials, it is clear that other defects (i.e., the C-rich layer) may also considerably contribute to leakage current generation and carrier recombination. It has also been demonstrated that to optimize the off-state leakage current of the SSi substrates a compromise has to be sought between the thickness of the SRB, on the one hand, and the relative position of the C-rich layer with respect to the junction depth, on the other.

4. Conclusions

It has been shown that the electrical characteristics of SSi wafers are strongly degraded by the presence of a high density of defects, compared with reference silicon wafers. The presence of the C-rich layer is believed to be a source of excess leakage current generation, whereby the impact strongly relies on its position relative to the p–n junction. For low off-state leakage applications at an operation voltage of 1 V, the C layer should be outside the maximum depletion region. This imposes a lower limit to the scaling of the SRB thickness: for the present well doping concentrations, the 348 nm layer is clearly superior compared with the 248 nm one, if an operation temperature of $\sim$100 °C is considered. A further thickness reduction can be accomplished by increasing the well doping density, although this enhances the electric field and associated leakage current mechanisms.

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